AF/2700 C/ #34

Atty.'s Docket No. 42390P4024

Patent

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Vishram P. Dalvi, et al.	Examiner: Robertson, D.
Serial No.: 08/814,928	Art Unit: 2187
Filing Date: February 27, 1997	
For: PROGRAMMING SUSPEND STATUS INDICATOR FOR FLASH MEMORY	

Assistant Commissioner for Patents
Washington, DC 20231

TRANSMITTAL COVER LETTER

Enclosed for filing in the U.S. Patent and Trademark Office, before the Board of Patent Appeals and Interferences are Appellant's Brief Pursuant to 37 C.F.R. 1.192(a), in triplicate and a check in the amount of $320.00 to cover the fee for filing the Appellant's Brief.

If there are any further charges not accounted for herein, please charge them to our deposit account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date Oct 17, 2001

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on October 17, 2001
Date of Deposit

Leah Resendez
Name of Person Mailing Correspondence

Leah Resendez 10-17-01
Signature Date

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Assistant Commissioner for Patents
Washington, DC 20231

APPEAL BRIEF
IN SUPPORT OF APPELLANTS' APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Dear Sir:

The Appellants hereby submit this Brief, in triplicate, in support of their appeal from a final decision of the Examiner mailed June 21, 2001 in the above-referenced application. The Appellants respectfully request consideration of this Appeal Brief by the Board of Patent Appeals and Interferences for allowance of the above referenced application.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

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REAL PARTY IN INTEREST

The real party in interest is Intel Corporation of Santa Clara, California, which is the assignee of the present patent application.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, the Appellants' legal representative, or assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

The above-mentioned application originally contained 29 claims. Claims 30-37 were added. Claims 1-30 are withdrawn from consideration. Claims 31-37 are pending in the application and set forth in the Appendix hereto. Claim 31 is an independent claim. Under the final rejection mailed on June 21, 2001, claims 31-37 remain rejected under 35 U.S.C. § 103(a) as being unpatentable over any one of applicants' admitted prior art or, U.S. Patent No. 5, 561,628 of Terada, et al. ("Terada"). Claims 31-37 reamain rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,937,424 of Leak et al. ("Leak") in view of Terada.

The Appellants appeal the above rejection regarding claims 31-37 with respect to the 35 U.S.C. § 103(a) rejections and hereby traverse every ground of rejection set forth in the final rejection.

STATUS OF AMENDMENTS

No amendment has been filed subsequent to final rejection. A Notice of Appeal From The Examiner to the Board of Patent Appeals and Interferences was filed from the decision dated June 21, 2001 of the Examiner rejecting claims 31-37.

SUMMARY OF INVENTION

The present invention is defined by claims 31-37 and their equivalents. The present section of this Appeal Brief is set forth merely to comply with the requirements of 37 C.F.R. § 1.192(c)(5) and is not intended to limit claims 31-37 in any way. See MPEP § 1206.

Claim 31 describes a memory device, comprising a control circuit coupled to a memory array and a register. The register is configured to store at least one bit indicating a suspend status of a write operation for the memory array. The control circuit is configured to update the register and to control the output of a status signal representing the suspend status of the write operation. The control circuit includes a first state machine (Command State Machine) to receive commands for accessing the memory array or said register, and a second state machine (Write State Machine) coupled to the first state machine to execute the commands received by said first state machine. (See specification pg. 9, ln. 15 through pg. 15, ln. 7, and Figure 3).

One embodiment of the memory device allows suspension of a programming operation at one memory location of the memory array in order to read data from another location of the memory array. A programming operation is suspended by entering a programming suspend command into the first state machine using standard microprocessor write timings. The contents of the first state machine serves as an input to the second state machine. A programming suspend command causes the second state machine to suspend the programming sequence at a predetermined point. (See specification pg. 16, lns. 6-14).

In one embodiment, the data operations of writing or programming data into the memory arrays are performed in byte increments. (See specification pg. 12, lns. 17-19). For one embodiment, a programming operation is referred to as a byte write operation. (See specification pg. 16, lns. 9-10). Claim 32 describes the memory device of claim 31, wherein said write operation represents a byte write operation.

One embodiment of the memory device operates in the byte write suspend mode which enables the system to read data or execute code from any other memory location within the memory array while the byte write operation is suspended. (See specification pg. 12, lns. 21-24). The status register may also provide a byte write suspend status signal that indicates whether a byte write operation has been suspended. (See specification pg. 14, lns. 8-10). Claim 33 describes the memory device of claim 31, wherein said status signal represents a byte write suspend command.

The CPU may access the data stored in the register by providing a signal to the first state machine that provides a "read status register" command to the register. The register outputs the requested status data. (See specification pg. 14, lns. 14-18). For one embodiment the register store byte write suspend information that indicates whether the programming operation is suspended or not suspended in response to the programming suspend command. (See specification pg. 16, lns. 14-16). Claim 34 describes the memory device of claim 31, wherein said control circuit is to receive a status request signal and said register is to output said status signal in response to said status request signal, said status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended. Claim 36 describes the memory device of claim 31, further comprising a status output coupled to said register, wherein said status output is to provide a second status signal if said status output is polled, and wherein said second status signal

having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

In one embodiment the CPU accesses the data stored in the register over a data bus coupled to data input/output pins. The data bus is coupled to the first state machine of the memory device. In response to a "read status register" command from the CPU, the first state machine provides a "read status register" signal to the register. The register outputs the requested status data from the memory device to the CPU. (See specification pg. 12, lns. 1-3, pg.14, lns. 14-22, and Figure 3). Claim 35 describes the memory device of claim 31, further comprising at least one data input/output coupled to said control circuit, wherein the at least one data input/output is to receive said status request signal from a processor and to provide said status signal to said processor. Claim 37 describes the memory device of claim 31, wherein said status request signal is a read status register command.

ISSUES

A. Whether under 35 USC §103(a) claims 31-37 are unpatentable in view of applicants' admitted prior art ("AAPA") and Terada.

B. Whether under 35 U.S.C. §103 (a) claims 31-37 are unpatentable in view of Leak and Terada.

GROUPING OF CLAIMS

For the purpose of the rejection of claims 31-37 under 35 U.S.C. § 103(a) in view of applicant's admitted prior art and Terada, and for the purpose of the rejection of claims 31-37 under 35 U.S.C. § 103(a) in view of Leak and Terada, claims 31-37 stand together.

ARGUMENTS

Under the final rejection mailed on June 21, 2001, claims 31-37 remain rejected under 35 U.S.C. § 103(a) as being unpatentable in view of applicant's admitted prior art and Terada and claims 31-37 remain rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Leak and Terada. In assessing obviousness under 35 U.S.C. § 103(a), inquiries should be made into the scope and content of the prior art and the differences between the claimed invention and the prior art.

The scope and content of the cited prior art.

The final obviousness rejection of claims 31-37 was based on the references of applicants' admitted prior art ("AAPA"), Terada, and Leak.

AAPA discloses the use of status registers to store status information relating to the internal operations of a flash memory device. The status register may store information indicative of whether a memory operation (e.g., read, write or erase) is in progress or completed. The register may store information that indicates whether the operation was completed successfully or not, as well. The AAPA also disclosees the status register data being output in response to a read status register command. (Spec. p.1, lines 7-14). AAPA also disclosees that the overall performance of a flash memory device may be improved through the suspension of an erase operation (i.e., the processor may read or write data at a

different memory location rather than waiting for the completion of the erase operation in progress) (Spec. p.1 line 26 – p. 2 line 2).

Terada discloses an IC card having a plurality of flash memory devices and a card interface. The card interface includes a test circuit. Terada discloses a testing method for the flash memory devices after they have been mounted on the IC card. The test method of Terada allows for a test signal via the card interface to the plurality of flash memory devices. The method allows for a parallel writing operation or parallel erasing operation. Terada discloses the ability to suspend erase cycles and a status register that outputs an erase suspend status signal.

Leak discloses, a memory device that allows suspending a program operation. The memory device includes a memory array, a command register, and memory array control circuitry. The command register decodes a program suspend command and provides a suspend signal as an output. The memory array control circuitry is coupled to receive the suspend signal from the command register. The memory array control circuitry performs a program operation in which data is written to the memory array. The memory array control circuitry suspends the program operation upon receiving the suspend signal. Leak discloses that it is advantageous to be able to suspend both erase and write (program) operations.

The differences between the claimed invention and the prior art.

a. Applicants' Admitted Prior Art Teaches Away From the Claimed Invention

The AAPA discloses the possibility of improving the overall performance of a flash memory device through the suspension of an erase operation and a status register with an erase suspend status (ESS) indicator to indicate that if an erase operation was suspended.

However the AAPA clearly teaches away from the application of these concepts to a program operation.

The AAPA discloses that an erase operation takes much longer than a program operation. The AAPA compares the "few milliseconds" for an erase operation with the "7-8 microsecond" for a program operation, and the "85 nanoseconds" for a read operation. The AAPA draws a line with erase operations on one side and programming and read operations on the other.

> "Typically, an erase operation takes much longer time to complete as compared to a programming or read operation."

(U.S. Application Serial No.08/814,928, page 1, lines 21-22).

This is because a substantially larger number of read operations can be performed in the time required to perform one erase operation than in the time required to perform one programming operation. Moreover, as the AAPA makes clear, the overall performance of a flash memory device is improved through the suspension of an erase operation, because when the erase operation is suspended a program operation or a read operation may be completed. The specification states

> "Thus, when an erase operation to a specific memory location is suspended, the processor may *program or read* data from a different memory location rather than waiting for the completion of the current erase operation. The ability to suspend an *erase* operation may improve the overall performance of a flash memory device.

(U.S. Application Serial No. 08/814,928, p. 1, line 25 – p. 2, line 2) (Emphasis added).

Moreover, the Examiner attempts to downplay the significant difference in the time required to complete an erase operation compared to a programming operation as noted in the AAPA by citing Terada. Specifically the Examiner states that

> "However, while a programming operation does not take as long as an erase operation, it still takes a significant amount of time relative to a read operation. In a particular 8M-bit IC card it "takes one second or less to read all the addresses on (sic of) one flash memory, 9.6 seconds to write in all the addresses in one flash memory, and 25.6 seconds to erase from all the addresses of one flash memory..."""

(U.S. Patent and Trademark Office Action mailed 6/21/01, p. 4)

The Examiner's reliance on this teaching of Terada is flawed in two respects. First, the writing time (9.6s) and the erasing time (25.6s) are the times required to write in, and erase from, **all** the addresses in one flash memory. The fact that an erase operation for all the addresses in one flash memory takes approximately only two and one-half times as long as a write operation to all the addresses in one flash memory is not pertinent to the claimed subject matter. As noted in the AAPA an erase operation to a specific memory location make take several hundred times as long as a programming (write) operation. The specification states

> "Additionally, the processor in a system may want to know whether an erase operation *to a specific memory location* has been suspended. Typically, an erase operation takes much longer time to complete as compared to a programming or read operation. For example, an erase operation may take a few milliseconds, whereas a programming operation may take 7-8 microseconds and a reading operation may take 85 nanoseconds.

(U.S. Application Serial No. 08/814,928, p. 1, lines 19-25) (Emphasis added).

The second respect in which reliance on this teaching is flawed is that the comparison of Terada is being made not to show that read operations may be performed during suspension of erase operations thus improving memory performance, but to show that a substantial amount of time is used to write to, or erase, all the memory locations of a device

for testing purposes and that this time can be reduced by a parallel write operation or parallel erase operation. Terada states that

> "The time required for the writing processes and the erasing processes in the conventional test methods drastically increases in proportion with the number of devices, thereby greatly increasing the cost of examination for the IC card. It is difficult to realize parallel writing or parallel erasing by using a testing program too."

(Terada, Col. 5, lns. 21-27)

Terada discloses the comparison of the time required for a write operation to all memory locations with the time required for an erase operation to all memory locations in order to show that substantial time may be saved in testing through the use of parallel write and parallel erase operations. This teaching does not at all make clear or suggest that performance may be improved by completing read operations to a specific memory during the suspension of a programming operation to a different specific memory location as is the case with completing read operations to a specific memory during the suspension of an erase operation to a different specific memory location.

Thus, in its entirety, the AAPA can only be viewed as teaching away from the claimed subject matter despite the Examiner's citation of Terada. Therefore, appellants respectfully submit that it would not have been obvious to a person having ordinary skill in the art of the claimed subject matter to have modified the AAPA to include the ability to suspend program operations to improve the overall performance of a flash memory device.

b. Terada is not Analogous Prior Art

There are two criteria to determine if prior art is analogous (i.e., relevant to a consideration of obviousness under 103). The first is whether the art is from the same field

of endeavor. If not, the further consideration is whether the art is nonetheless reasonably pertinent to the particular problem addressed by the claimed subject matter.

The Examiner agrees that the field of endeavor of the claimed present invention is the improvement of the overall performance of a flash memory device. In particular the Examiner has stated that

> "It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said claimed subject matter pertains to have modified applicants' admitted prior art to include the ability to suspend program operations *to improve the overall performance of a flash memory device.*"

(U.S. Patent and Trademark Office Action mailed 6/21/01, p. 3) (emphasis added).

The Examiner also stated that

> "It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said claimed subject matter pertains to have modified the memories taught by Terada to include the ability to suspend programming operations *to improve the overall performance of a flash memory device.*"

(U.S. Patent and Trademark Office Action mailed 6/21/01, p. 4) (emphasis added).

The Examiner fails to explore the field of endeavor of Terada which has nothing to do with improving the performance of flash memory devices. To be sure, Terada relates to flash memory devices, but Terada and the claimed subject matter are not in the same field of endeavor merely because both relate to flash memory devices. The field of endeavor of Terada is the improved efficiency of testing flash memory devices by performing a parallel write process or a parallel erase process for all of the plurality of flash memory devices on a given card. (See Terada, Col. 5, lns. 57-65).

Therefore, because the claimed subject matter is concerned with improving the overall operating performance flash memory devices while Terada is concerned with efficient testing of flash memory devices, it is clear that the field of endeavor of the claimed subject matter differs from that of Terada.

The next inquiry is whether Terada is nonetheless reasonably pertinent to the particular problem addressed by the claimed subject matter. Recall that the claimed subject matter addressed the problem of flash memory performance by completing read operations during the suspension of a program operation. The processor is informed that a programming operation to a specific memory location is suspended and therefore the processor may request that a read operation to another memory location be performed while the programming operation is suspended.

The Examiner contends that Terada is pertinent to the problem addressed by the claimed subject matter because Terada teaches the ability to suspend erase cycles and a status register that outputs an erase suspend status signal. A closer examination shows that the teachings of Terada are not pertinent to the problem addressed by the claimed subject matter. Terada teaches the suspension of erase cycles in response to certain interim test results during testing of a flash memory device. Terada states

> "Thus, the CPU checks whether or not a command sequence error has occurred during the erasing. If the values of the registers SR.4 and SR.5 are both "1", it is determined that a command sequence error has occurred, and the process proceeds to step S147a. If the value of the register SR.4 is not "1" and/or the value of the register SR.5 is not "1", the process proceeds to step S148. At step S147a, the CPU of the test apparatus main body 60a terminates the erasing test process.

(Terada, Col.16, lns. 51-58)

Therefore the extent of Terada's teaching is that during an erasing test of a flash memory, if an erasing error is detected, the erasing operation will be suspended. Terada makes no suggestion that during erase operation suspension a read operation may be performed thereby improving the performance of the flash memory device. In fact since the erase suspension occurs during testing, the memory device is not even in operation.

Therefore the teachings of Terada are not pertinent to the problem addressed by the claimed subject matter and Terada is not analogous prior art.

c. Niether Applicants' Admitted Prior Art Nor Terada Teach or Disclose the Claimed Subject Matter

Appellants respectfully submit the claimed subject matter, for example as claimed in claim 31, as amended, is not obvious over the AAPA or Terada. For claim 31 to be rendered obvious, the AAPA or Terada must disclose or suggest each and every limitation of the claim. Claim 31 includes the following limitations:

31. A memory device, comprising:

a memory array;

a register to store at least one bit indicating a suspend status of a write operation for the memory array; and

a control circuit coupled to said memory array and said register, said control circuit to update said register and to control an output of a status signal representing said suspend status of said write operation, and wherein said control circuit includes:

a first state machine to receive commands for accessing said memory array or said register, and

a second state machine coupled to said first state machine and to execute the commands received by said first state machine.

(Claim 31)(emphasis added).

A distinction of claim 31 over the AAPA and Terada is a register to store at least one bit indicating a suspend status of a write operation for the memory array as recited in claim 31.

Figure 1 of appellants' disclosure shows a prior art status register 100 having a memory location 104 for an erase suspend status ("ESS") information. The prior art status register 100, however, does not disclose or suggest a register to store at least one bit indicating a suspend status of a write operation as recited in claim 31.

Furthermore, appellants respectfully submit that the Examiner has incorrectly applied obviousness to claim 31 with respect to the AAPA. In particular, the Examiner indicates that it would have been obviousness to incorporate the ability to suspend "programming operations" with the AAPA. (U.S. Patent and Trademark Office Action mailed 6/21/01, p.4). Claim 31, however, recites at least one bit of a register indicating a suspend status of a write operation.

Terada, in Figure 1, discloses an IC card having flash memories 40a and 40d with a status register 41. Status register 41 includes 8 bits in which bit 6 indicates a status for an "erase suspend" status. Claim 31, however, recites a register to store at least one bit indicating a suspend status of a write operation.

Furthermore, appellants respectfully submit that the Examiner has incorrectly applied obviousness to claim 31 with respect to Terada. In particular, the Examiner indicates that it would have been obviousness to incorporate the ability to suspend "programming operations" with Terada. (U.S. Patent and Trademark Office Action Mailed 6/21/01, pg. 3, lns. 1-4).

Claim 31, however, recites at least one bit of a register indicating a suspend status of a write operation.

Therefore, neither the AAPA nor Terada individually or in combination disclose or suggest the above distinction of claim 31.

Another distinction of claim 31 over the AAPA and Terada is a control circuit coupled to said memory array and said register, and said control circuit to update said register and to control an output of a status signal representing said suspend status of said write operation.

Figure 1 of appellants' disclosure does not show a control circuit as recited in claim 31. Instead, Figure 1 shows a prior art status register 101 with five status locations, and one of the locations is for an "erase suspend" status. Terada, however, does not disclose a control circuit that outputs a status signal representing a suspend status of a write operation as recited in claim 31. Terada, like the AAPA, discloses a suspend status for an erase operation and not a write operation as recited in claim 31.

As discussed above the AAPA teaches away from a status signal representing a suspend status of a programming operation, and Terada provides no suggestion for including such. Therefore, neither the AAPA nor Terada individually or in combination disclose or suggest the above distinction of claim 31.

d. Terada in Combination With Leak Fails to Teach or Disclose the Claimed Subject Matter

Appellants respectfully submit the claimed subject matter, for example as claimed in claim 31, as amended, is not obvious over Leak in view of Terada. For claim 31 to be rendered obvious, Leak and Terada must individually or in combination teach each and

every limitation of claim 31. Furthermore, there must be some motivation or suggestion to combine Leak with Terada.

Appellants respectfully submit that the above distinctions of claim 31 noted above are also distinctions over Leak in view of Terada.

In particular, Leak discloses in FIG. 6 a status register 142. Leak, however, does not teach or suggest a register having a bit indicating a suspend status of a write operation as recited in claim 31, which the Examiner admits. Furthermore, Leak discloses a command decoder 170 to clear command latches 176a-n. Leak does not disclose a control circuit to update a register and to control an output of a status signal representing said suspend status of said write operation as recited in claim 31.

Terada fails to cure the deficiencies of Leak. As noted previously, Terada discloses a status register 41 having 8 bits in which bit 6 indicates a status for an "erase suspend." Terada, however, does not teach or suggest status register 41 having a bit for "suspend status" of a "write operation".

It is also respectfully submitted neither Terada nor Leak provide any motivation or suggestion to combine one with the other. When viewed in its entirety, Terada, which is concerned with improving the efficiency of testing flash memory devices, has nothing to do with Leak, which concerns suspending a write operation in order to perform a read operation. There is no suggestion to combine Leak with Terada. Appellants' respectfully submit that it would be impermissible hindsight based on appellants' own disclosure to incorporate Leak with Terada. Moreover, even if Leak and Terada are combinable, such a combination would still fail to disclose or suggest the status register as recited in claim 31.

SUMMARY

In summary, Appellants contend that claims 31-37 are distinguished over AAPA and Terada. Appellants contend further that claims 31-37 are distinguished over Leak in view of Terada. Therefore, Appellants respectfully submit that all appealed claims in this application are patentable and requests that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

FEE FOR FILING A NOTICE TO APPEAL

A check in the of $320.00 to cover the fee for filing a Notice of Appeal required under 37 C.F.R. § 1.17(e) was previously submitted with a prior Notice of Appeal filed on August 23, 2001. The Notice of Appeal was filed within the three month time period given for response to the outstanding office action and therefore not extension of time was required.

FEE FOR FILING A BRIEF IN SUPPORT OF APPEAL

Enclosed is a check in the amount of $320.00 to cover the fee for filing of a brief in support of an appeal required under 37 C.F.R. § 1.17(c) and 1.192.

CHARGE OUR DEPOSIT ACCOUNT

If there are any further charges not accounted for herein, please charge them to our deposit account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date Oct 17, 2001

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APPENDIX

The claims involved in the appeal follow.

31. (Three Times Amended) A memory device, comprising:

a memory array;

a register to store at least one bit indicating a suspend status of a write operation for the memory array; and

a control circuit coupled to said memory array and said register, said control circuit to update said register and to control an output of a status signal representing said suspend status of said write operation, and wherein said control circuit includes:

a first state machine to receive commands for accessing said memory array or said register, and

a second state machine coupled to said first state machine and to execute the commands received by said first state machine.

32. (Unchanged) The memory device of claim 31, wherein said write operation represents a byte write operation.

33. (Amended) The memory device of claim 31, wherein said status signal represents a byte write suspend command.

34. (Unchanged) The memory device of claim 31, wherein said control circuit is to receive a status request signal and said register is to output said status signal in response to said status request

signal, said status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

35. (Amended) The memory device of claim 31, further comprising:

at least one data input/output coupled to said control circuit, wherein the at least one data input/output is to receive said status request signal from a processor and to provide said status signal to said processor.

36. (Unchanged) The memory device of claim 31, further comprising:

a status output coupled to said register, wherein said status output is to provide a second status signal if said status output is polled, and wherein said second status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

37. (Unchanged) The memory device of claim 31, wherein said status request signal is a read status register command.